

Hardware Unit Test Report

Set-Top Box

T99X171T00

eMMC Flash Timing Test

Hardware version	FW version	Sample No.	eMMC Flash P/N
V005	4.9.113 #2 Wed Jan 30 17:12:43 CST 2019	S/N:	KLM8G1GETF-B041

Command:

*eMMC Read/Write測試指令

write 1G

```
time sh -c "dd if=/dev/zero of=/data/tmp.dd bs=1000k count=1000; sync"
```

read 1G

```
time sh -c "dd if=/dev/block/data of=/dev/zero bs=1000k count=1000; sync"
```

read 8G

```
time sh -c "dd if=/dev/block/data of=/dev/zero bs=1000k count=8000; sync"
```

1. eMMC Flash Timing Test

1.1 HS200 Timing Specification

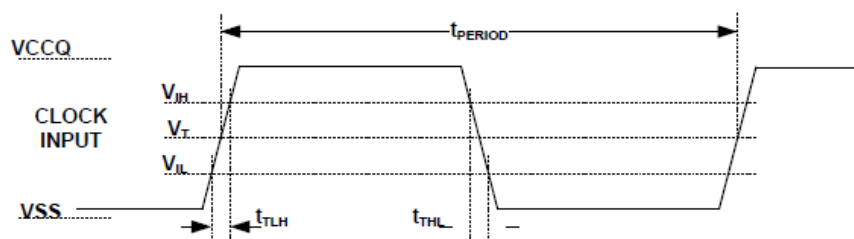
10.7 Bus Timing Specification in HS200 mode

10.7.1 HS200 Clock Timing

Host CLK Timing in HS200 mode shall conform to the timing specified in Figure 69 and Table 170.

CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device.

The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.



NOTE 1 V_{IH} denote $V_{IH(min)}$ and V_{IL} denotes $V_{IL(max)}$.

NOTE 2 $V_T=0.975V$ - Clock Threshold ($V_{CCQ} = 1.8V$) and $V_T=0.65V$ - Clock Threshold ($V_{CCQ} = 1.2V$), indicates clock reference point for timing measurements.

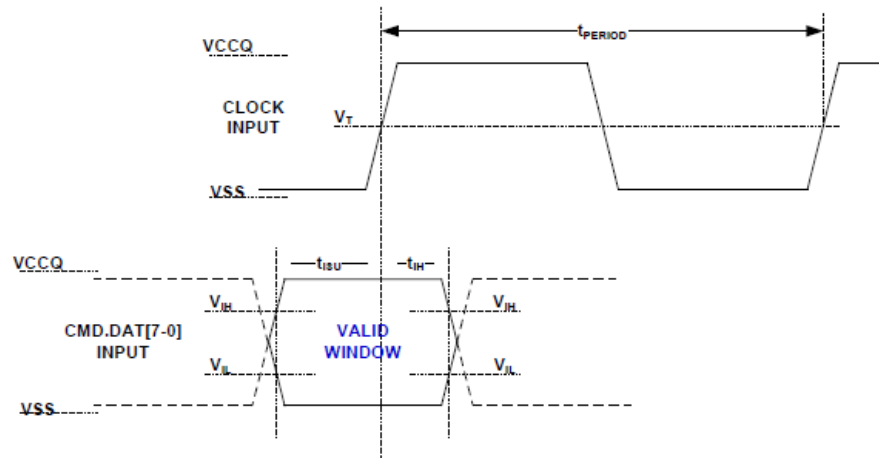
Figure 69 — HS200 Clock signal timing

Table 170 — HS200 Clock signal timing

Symbol	Min.	Max.	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	$0.2 \cdot t_{PERIOD}$	ns	$t_{TLH}, t_{THL} < 1ns$ (max.) at 200MHz, $C_{BGA}=12pF$, The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

10.7.2 HS200 Device Input Timing

Figure 70 and Table 171 define Device input timing.



Note1: t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
Note2: V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 70 — HS200 Device input timing

Symbol	Min.	Max.	Unit	Remark
t _{ISU}	1.40	-	ns	5pF≤C _{BGA} ≤12pF
t _{IH}	0.8		ns	5pF≤C _{BGA} ≤12pF

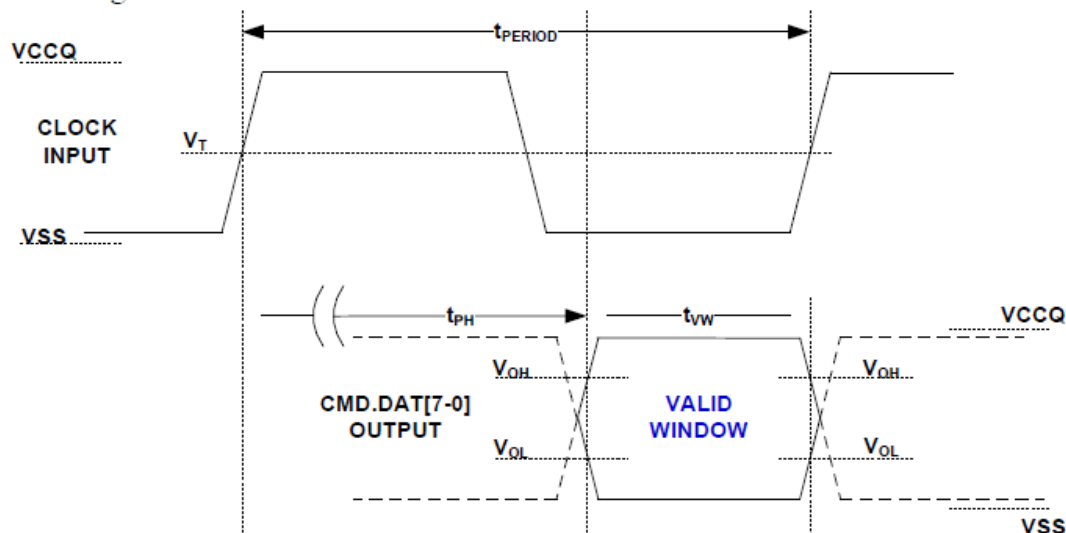
Table 171 — HS200 Device input timing

10.7.3 HS200 Device Output Timing

t_{PH} parameter is defined to allow device output delay to be longer than t_{PERIOD} . After initialization, the t_{PH} may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode.

Figure 71 and Table 172 define Device output timing.

While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by ΔT_{PH} . Output valid data window (t_{VW}) is available regardless of the drift (ΔT_{PH}) but position of data window varies by the drift, as described in Figure 72.



NOTE V_{OH} denotes $V_{OH(min.)}$ and V_{OL} denotes $V_{OL(max.)}$.

Figure 71 — HS200 Device output timing

Table 172 — Output timing

Symbol	Min.	Max.	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 ($\Delta T = -20$ deg.C)	+1550 ($\Delta T = 90$ deg.C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25 deg.C to 125 deg.C during operation.
t_{VW}	0.575	-	UI	$t_{VW} = 2.88ns$ at 200MHz Using test circuit in Figure 72 including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected T_{VW} at Host input is larger than 0.475UI.

NOTE Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.

1UI=5ns, ex: 720ps=0.72ns/5ns=0.144

1.2 Bus Signal Level

10.4 Bus signal levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

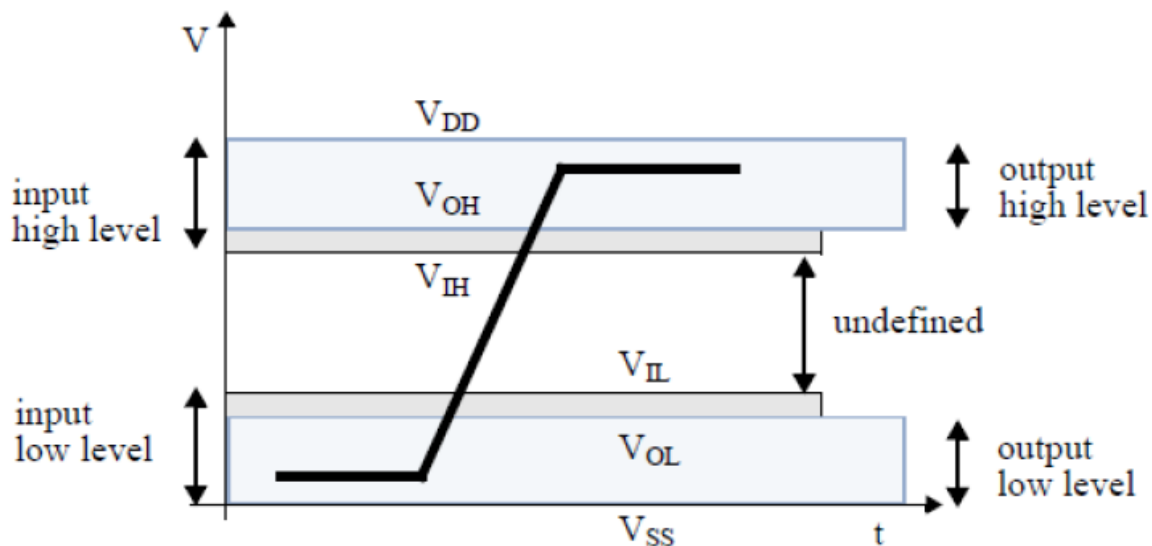


Figure 65 — Bus signal levels

Table 163 — Push-pull signal level—1.70 -1.95 VCCQ voltage Range

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	$V_{CCQ} - 0.45V$		V	$I_{OH} = -2mA$
Output LOW voltage	VOL		0.45V	V	$I_{OL} = 2mA$
Input HIGH voltage	VIH	$0.65 * V_{CCQ} (1)$	$V_{CCQ} + 0.3$	V	
Input LOW voltage	VIL	$V_{SS} - 0.3$	$0.35 * V_{DD}(2)$	V	

(1) $0.7 * V_{DD}$ for MMC4.3 and older revisions.

(2) $0.3 * V_{DD}$ for MMC4.3 and older revisions.

VOH=1.36V

VIL=620mV

1.3 Test Result and picture**1.3.1 Input Timing**

Test Item		Specification		Result	Unit	Pass / Fail
Symbol	Parameter	Minimum	Maximum			
Input CLK						
t _{PERIOD}	Cycle time data transfer mode	5	-	5.0	ns	Pass
t _{TLH}	Clock rise time	-	0.2* t _{PERIOD}	0.48	ns	Pass
t _{THL}	Clock fall time	-	0.2* t _{PERIOD}	0.48	ns	Pass
Duty Cycle	Clock Duty Cycle	30	70	40	%	Pass
Input DAT (reference to Clock)						
t _{ISU}	Input set-up time - D4	1.4	-	2.72	ns	Pass
t _{IH}	Input hold time - D4	0.8	-	2.24	ns	Pass
t _{ISU}	Input set-up time - D0	1.4	-	2.64	ns	Pass
t _{IH}	Input hold time - D0	0.8	-	1.28	ns	Pass
t _{ISU}	Input set-up time - CMD	1.4	-	2.8	ns	Pass
t _{IH}	Input hold time - CMD	0.8	-	2.16	ns	Pass

Note: D4 is the longest trace, D0 is the shortest trace

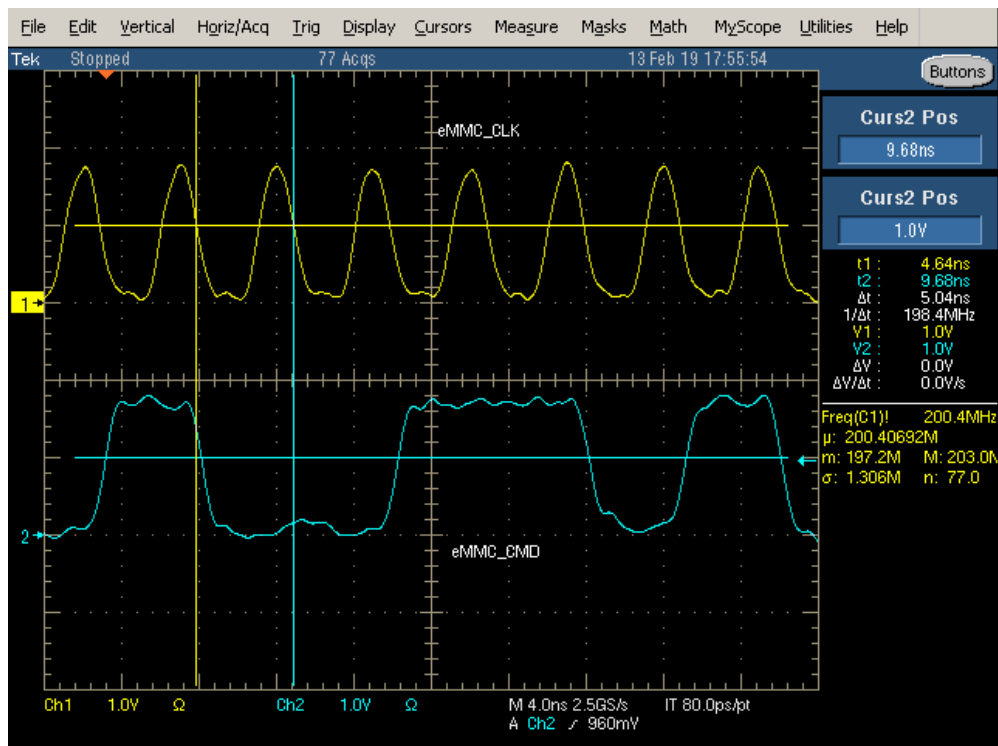
1.3.2 Output Timing

Test Item		Specification		Result	Unit	Pass / Fail
Symbol	Parameter	Minimum	Maximum			
Output DAT (reference to Clock)						
tPH	Momentary phase - D4	0	2	0.144	UI	Pass
tvw	Output valid window -D4	0.575	-	17.04	UI	Pass
tPH	Momentary phase – D0	0	2	0.144	UI	Pass
tvw	Output valid window –D0	0.575	-	1.04	UI	Pass
tPH	Momentary phase - CMD	0	2	0.416	UI	Pass
tvw	Output valid window -CMD	0.575	-	1.008	UI	Pass

1.3.3 Picture of input timing

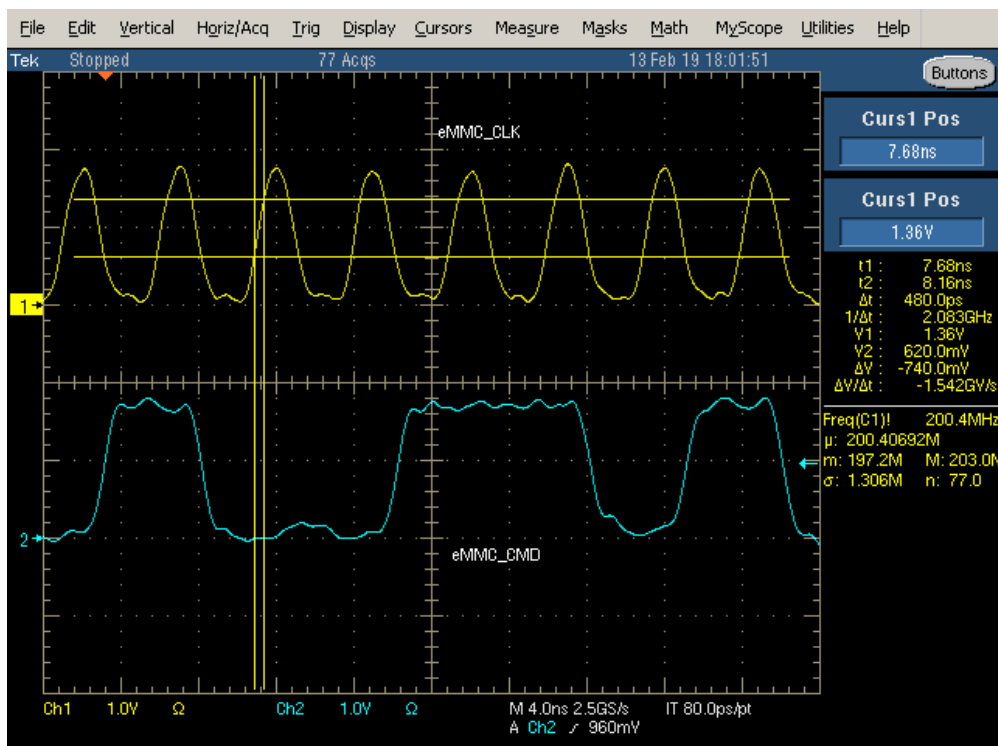
1.3.3.1 Input CLK - tPERIOD

Symbol	Parameter	Minimum	Maximum	Result	Result
t _{PERIOD}	Cycle time data transfer mode	5ns	—	5.0ns	Pass



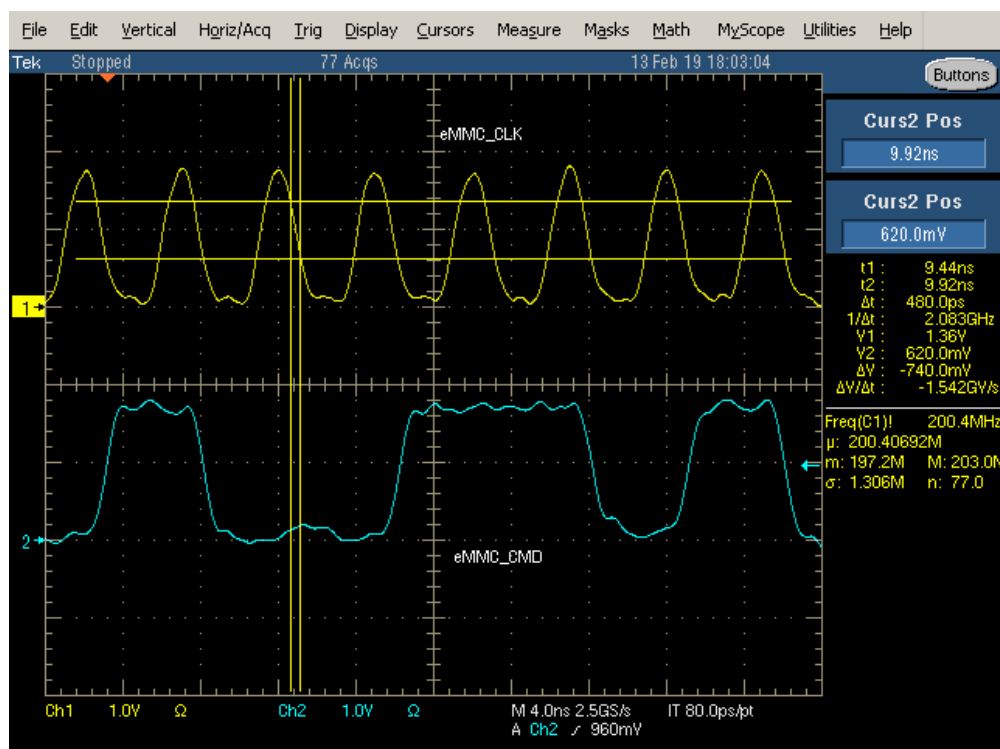
1.3.3.2 Input CLK - t_{TLH} (Clock rise time)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t _{TLH}	Clock rise time	-	0.2* t _{PERIOD}	0.48ns	Pass

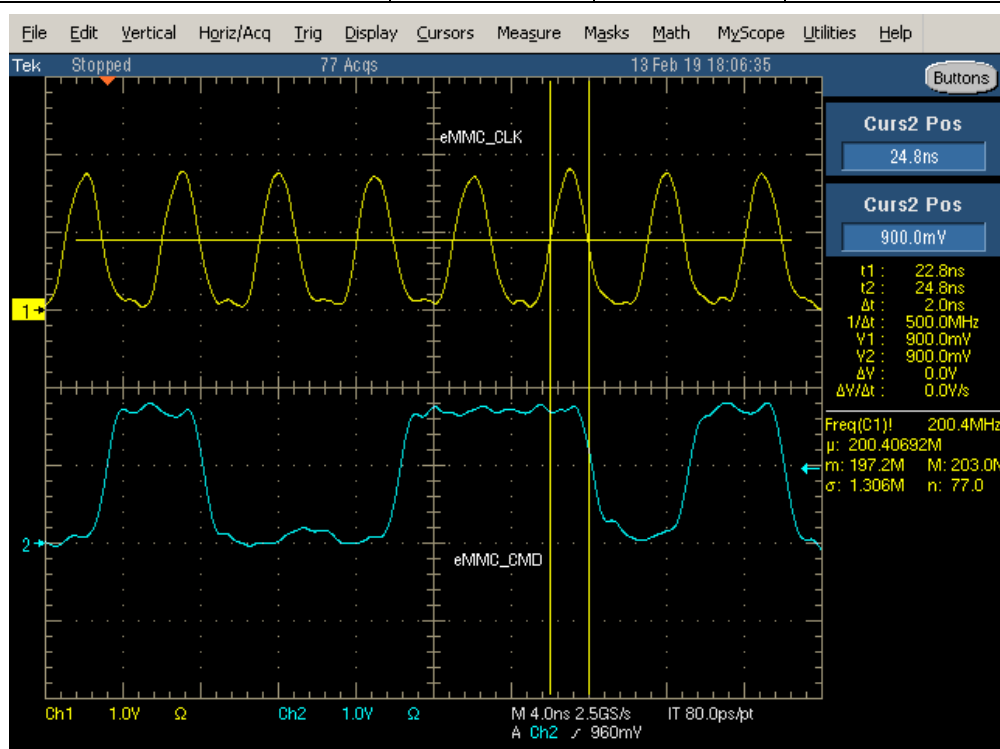


1.3.3.3 Input CLK - t_{THL} (Clock fall time)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t _{THL}	Clock fall time	-	0.2* t _{PERIOD}	0.48ns	Pass

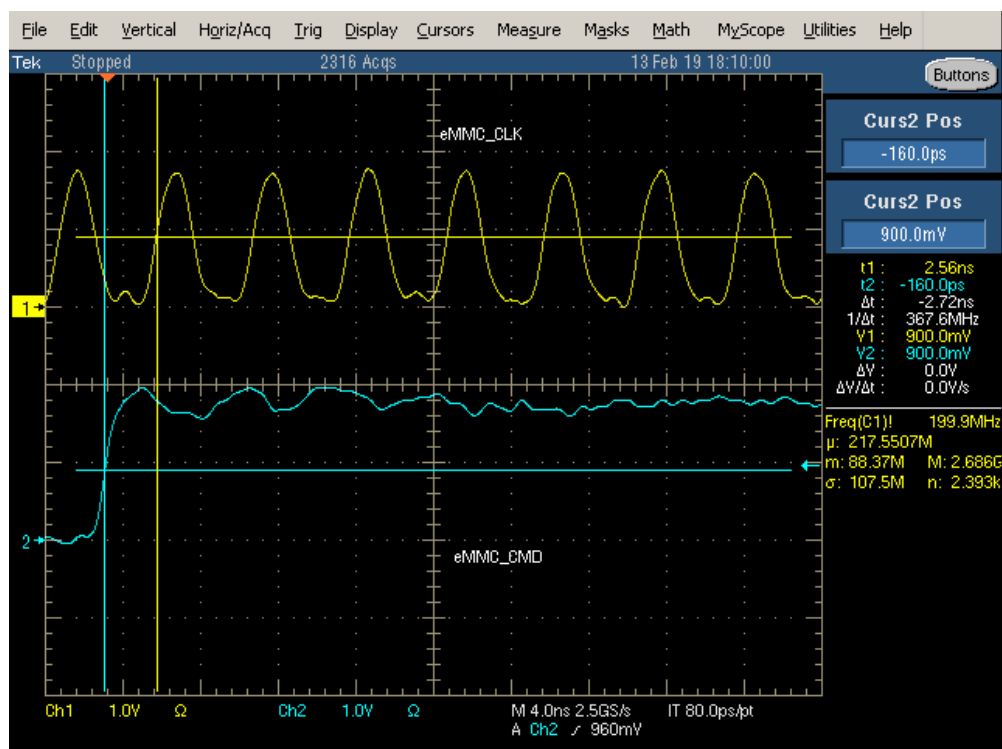
**1.3.3.4 Input CLK – Duty Cycle (Clock Duty Cycle)**

Symbol	Parameter	Minimum	Maximum	Measurement	Result
Duty Cycle	Clock Duty Cycle	30	70	40%	Pass



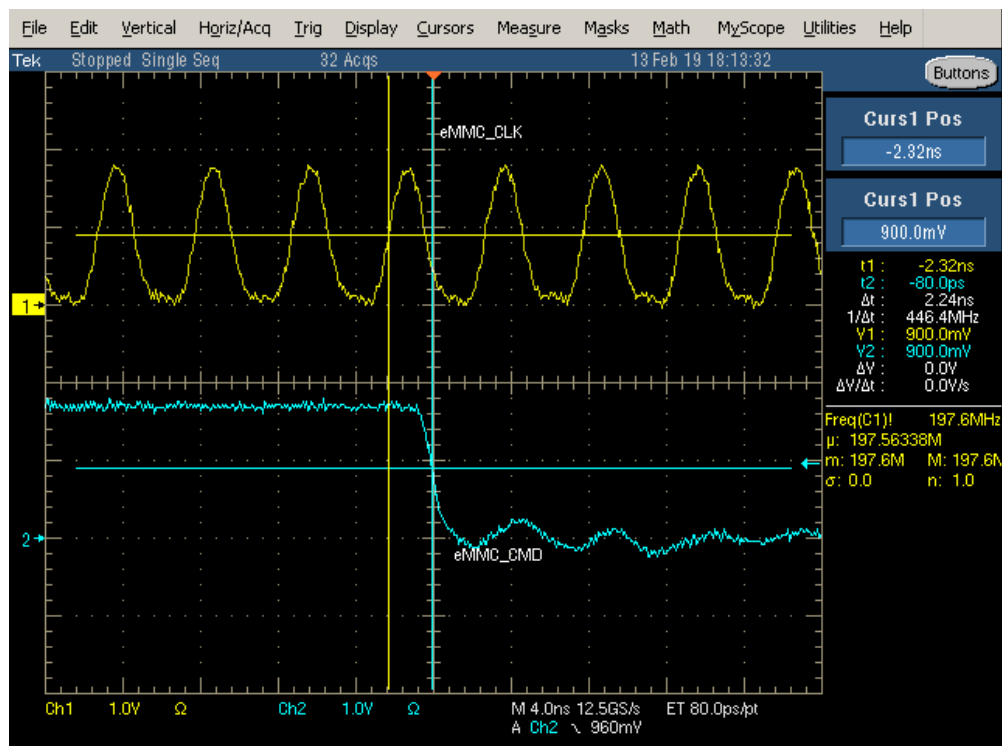
1.3.3.5 Input Set-up time (D4)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t _{isu}	Input set-up time	1.4ns	-	2.72ns	Pass



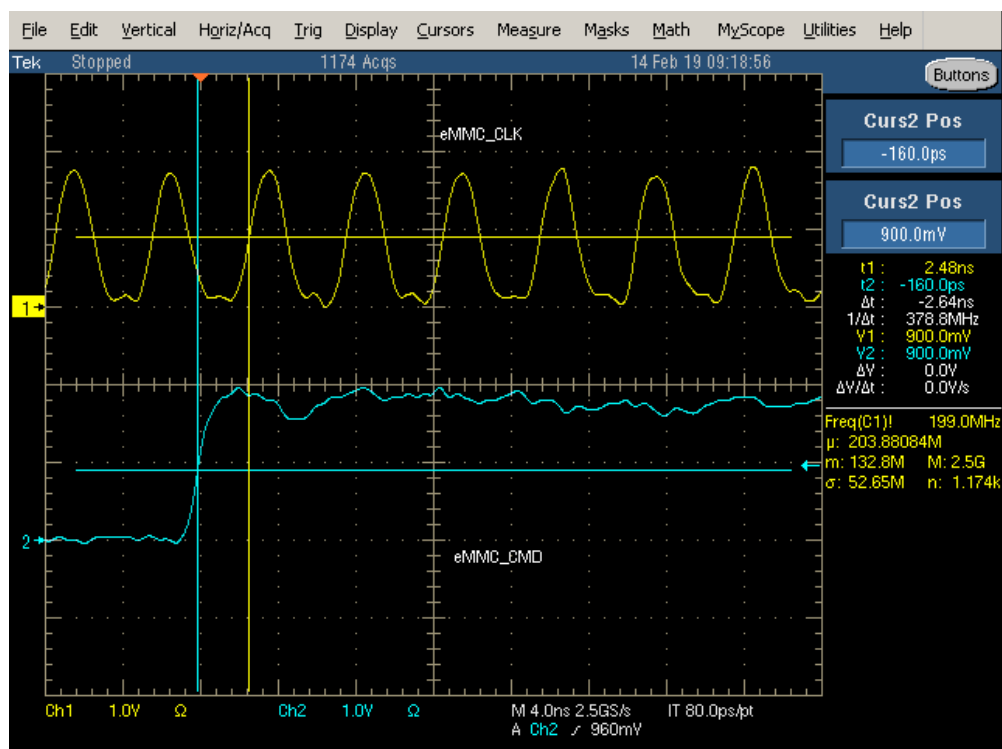
1.3.3.6 Input hold time (D4)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t _{IH_patch}	Input hold time	0.8ns	-	2.24ns	Pass



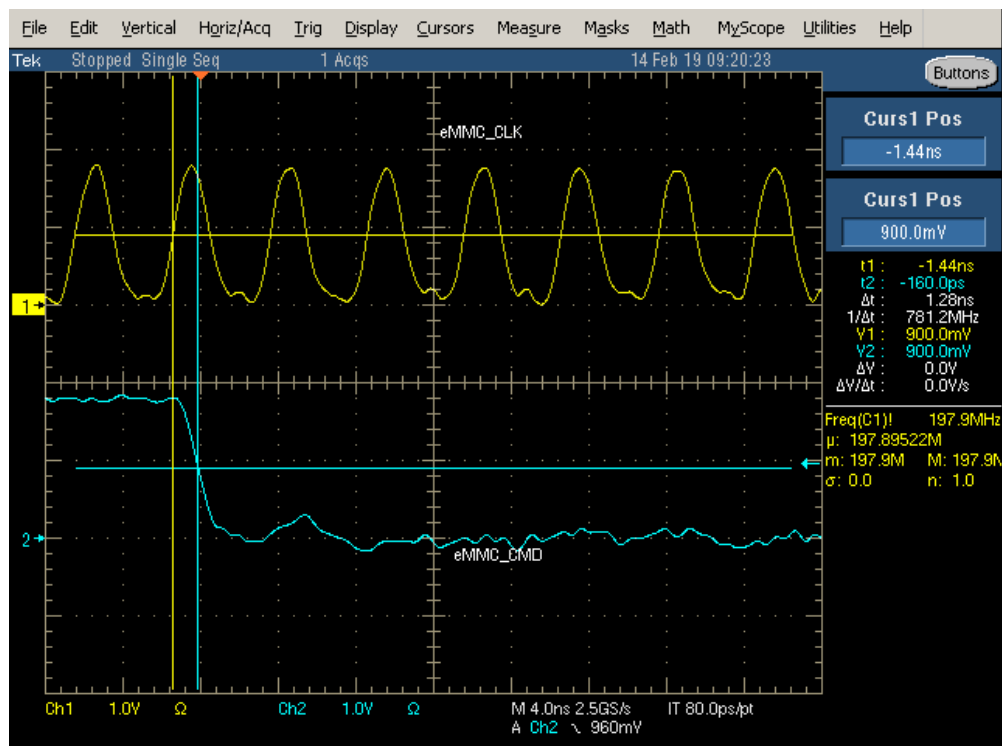
1.3.3.7 Input Set-up time (D0)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t _{isu}	Input set-up time	0.4ns	-	2.64ns	Pass



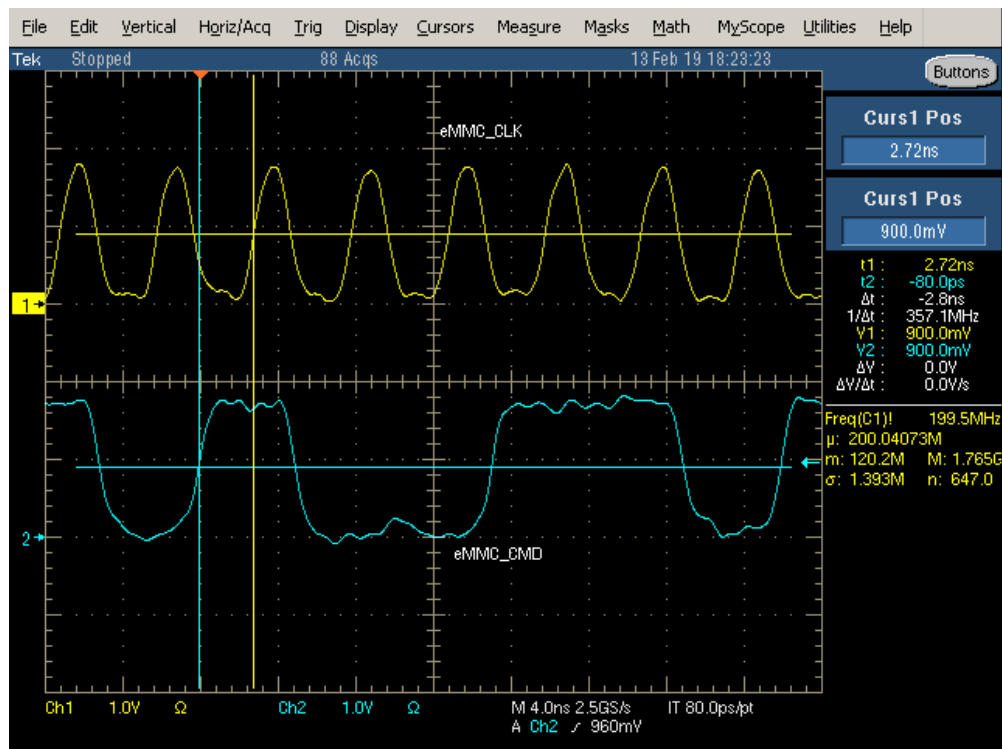
1.3.3.8 Input hold time (D0)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
T _{IHddr}	Input hold time	0.8ns	-	1.28ns	Pass



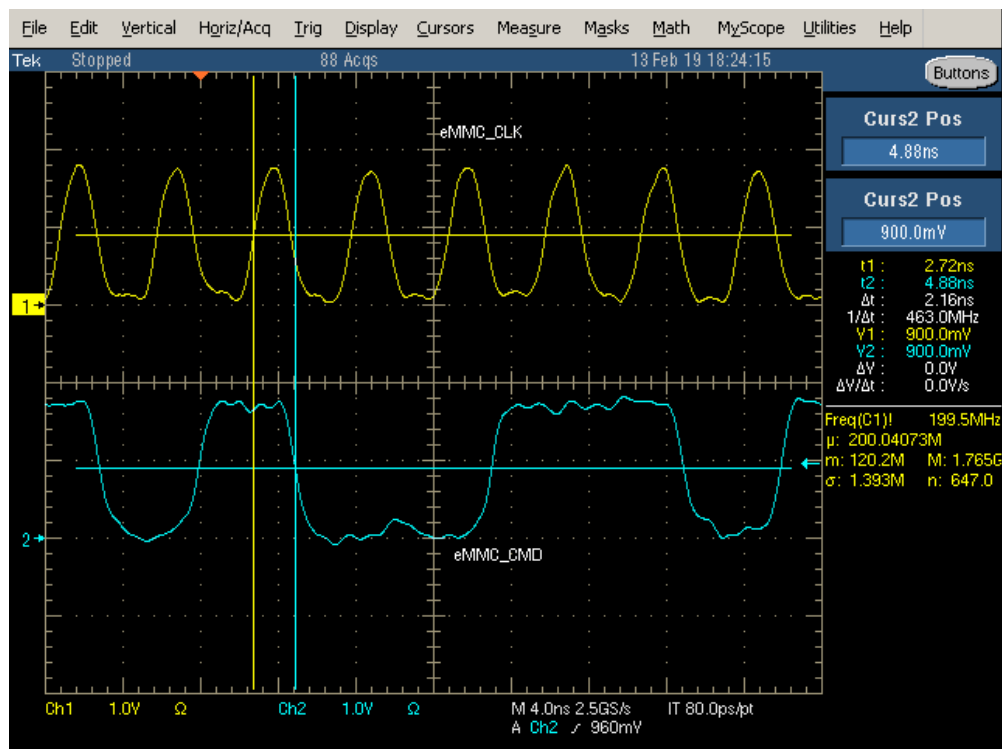
1.3.3.9 Input Set-up time (CMD)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t _{isu}	Input set-up time	1.4ns	-	2.8ns	Pass



1.3.3.10 Input hold time (CMD)

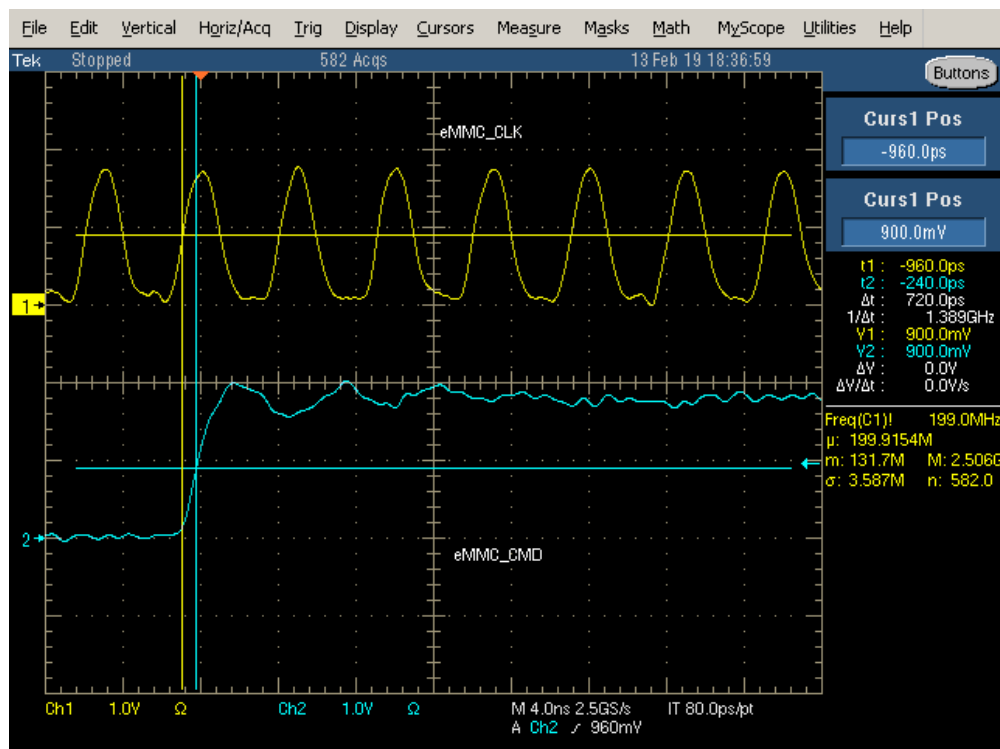
Symbol	Parameter	Minimum	Maximum	Measurement	Result
T _{IHddr_patch}	Input hold time	0.8ns	-	2.16ns	Pass



1.3.4 Picture of Output Time

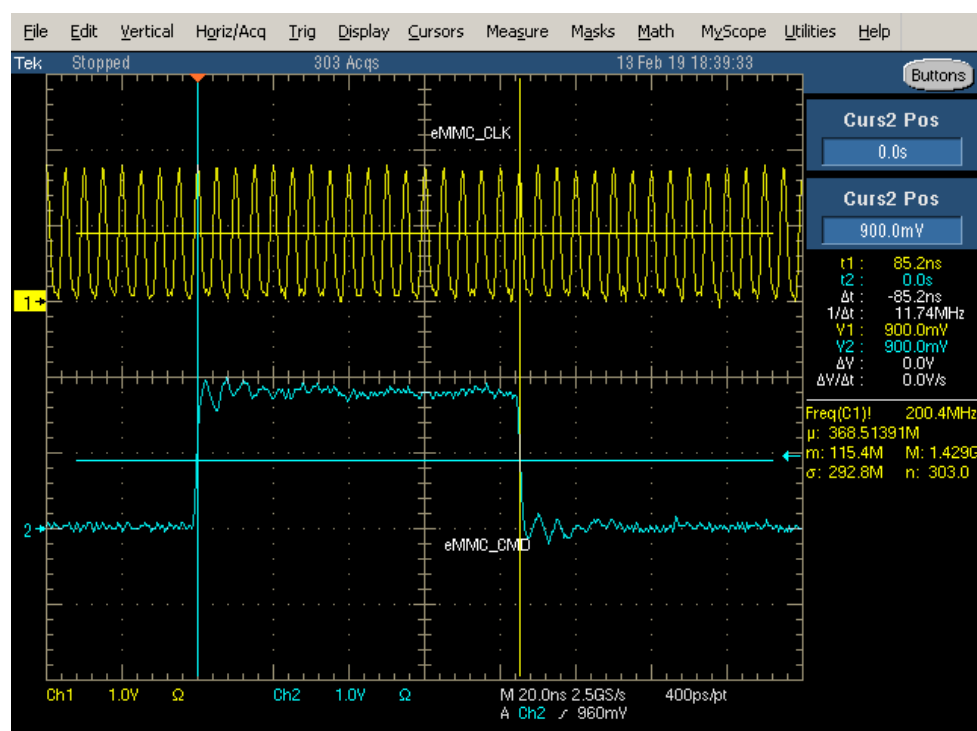
1.3.4.1 D4 – t_{PH} (Momentary phase)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t_{PH_patch}	Momentary phase	0	2	0.144 UI	Pass



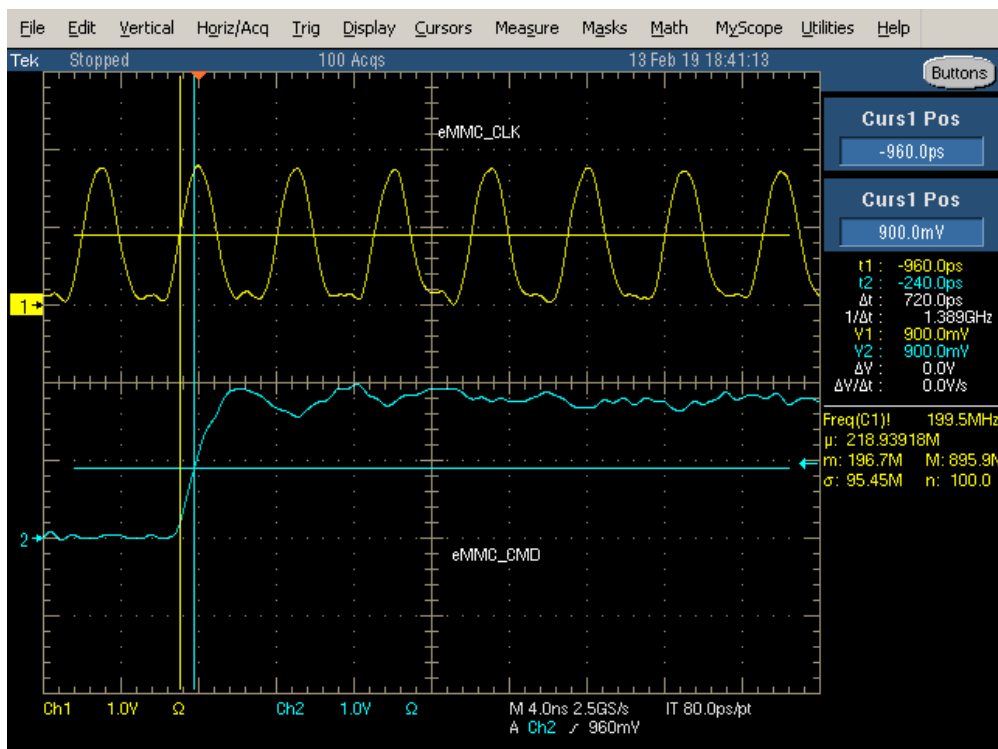
1.3.4.2 D4 - t_{w} (Output valid window)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t_{w_patch}	Output valid window	0.575	-	17.04UI	Pass

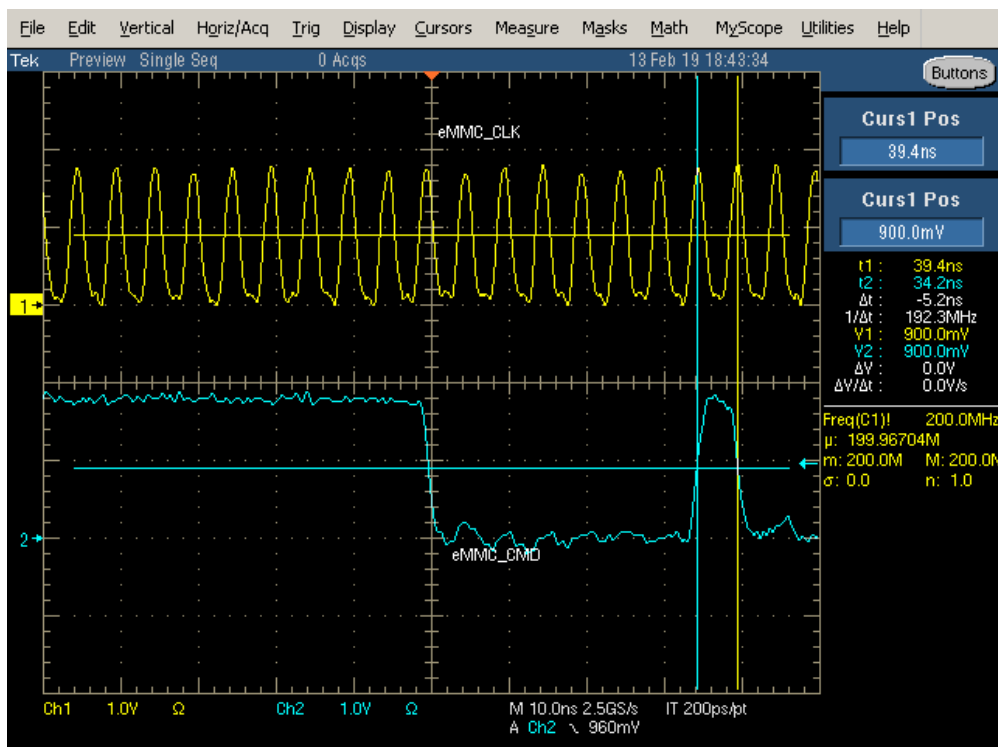


1.3.4.3 D0 – t_{PH} (Momentary phase)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t _{PH_patch}	Momentary phase	0	2	0.144 UI	Pass

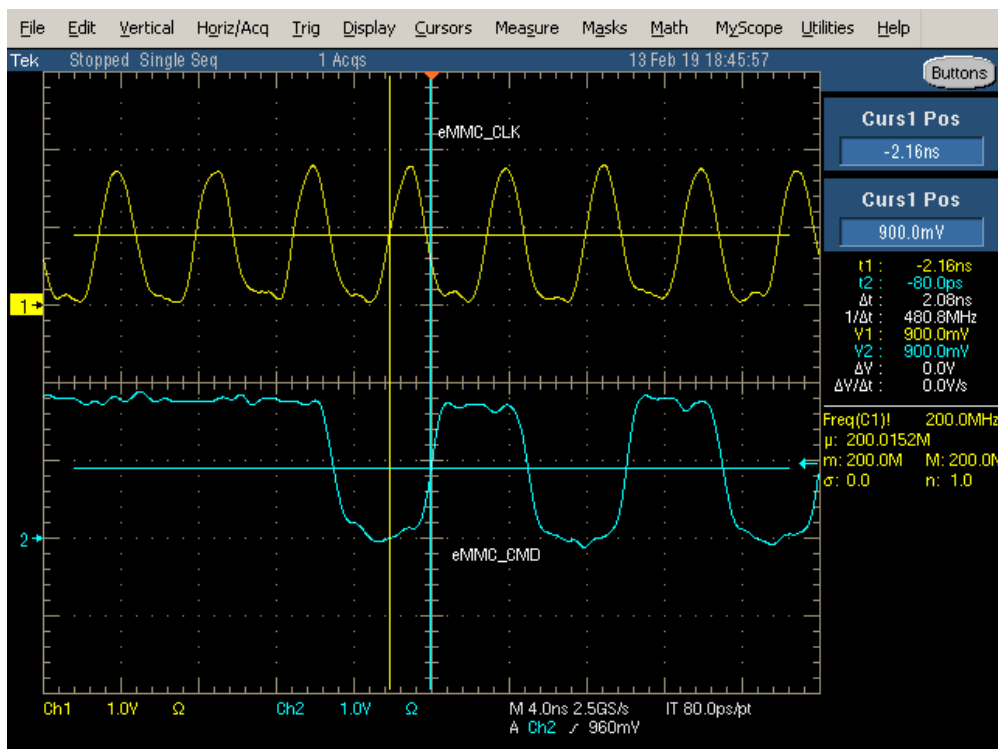
1.3.4.4 D0 - t_{vw} (Output valid window)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t _{vw_patch}	Output valid window	0.575	-	1.04 UI	Pass



1.3.4.5 CMD – t_{PH} (Momentary phase)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t_{PH_patch}	Momentary phase	0	2	0.416 UI	Pass

1.3.4.6 CMD - t_{vw} (Output valid window)

Symbol	Parameter	Minimum	Maximum	Measurement	Result
t_{vw_patch}	Output valid window	0.575	-	1.008 UI	Pass

